REMARKS

This Amendment is in response to the Office Action mailed 04/28/2005. In the Office Action, the Examiner rejected claims 1-25 under 35 U.S.C. § 103. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 103

3. The Examiner rejects claims 1-2, 6-7, 11-12, and 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Isaka (US 6,654,455) in view of Iwama et al. (US 6,600,735).

Applicant has cancelled all claims and presents new claims 26-50. Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-2, 6-7, 11-12, and 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Iwama.

4. The Examiner rejects claims 3, 8, 13, 19, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Isaka (US 6,654,455) in view of Iwama et al. (US 6,600,735), and further in view of Onishi et al. (US 5,434,863).

As to claim 3, the Examiner admits that Isaka fails to teach the method of claim 1, wherein the descriptor fields include a memory pointer field, status field, mask field, or a data length field. The Examiner asserts that Onishi teaches the descriptor fields include a memory pointer field, status field, mask field, or a data length field citing a field 401 of an IP address for representing the destination network and subnet mask data 402 for representing subnet information of the destination network. Applicant respectfully submits that neither of these fields taught by Onishi is a memory pointer field, status field, mask field, or a data length field as those terms are defined by paragraphs [0029] and [0030] of the specification.

As to claims 8, 13, 19, and 23, the Examiner asserts that these claims do not teach or define any new element above claims 1-2 and the Examiner rejects these claims for similar reasons as claim 3. Applicant likewise traverses the rejections for similar reasons.

Applicant has cancelled all claims and presents new claims 26-50. Applicant respectfully requests that the Examiner withdraw the rejection of claims 3, 8, 13, 19, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Iwama, and further in view of Onishi.

5. The Examiner rejects claims 4-5, 9-10, 14, and 24-25 under 35 U.S.C. § 103(a) as being unpatentable over Isaka (US 6,654,455) in view of Iwama et al. (US 6,600,735), in view of Onishi et al. (US 5,434,863), and further in view of Lin et al. (US 6,651,225).

As to claim 4, the Examiner admits that Isaka fails to teach using a multicast hardware accelerator to send the voice data to selected user devices based on the mask field. The Examiner asserts that Lin teaches a hardware accelerator citing item 120 of Figure 2. Lin teaches a dynamic logic evaluation system. Applicant respectfully submits that Lin is non-analogous art and that one of ordinary skill in the art would not be motivated to consider the teachings of Lin in connection with voice communication.

The hardware accelerator taught by Lin is a modeling of a circuit design where the model is implemented in hardware, such as a FPGA. The hardware model is used as an alternative to software simulation for portions of the cycles being modeled for the circuit design. Col. 15, line 57, through Col. 19, line 14. Nothing in Lin teaches or suggests "a multicast hardware accelerator to multicast the voice data stored in the buffer memory to ports selected from the plurality of ports by a single voice packet received from the host system" as now claimed.

The Examiner asserts that one would have been motivated to modify Isaka to provide the hardware accelerator of Lin to allow multiple users doing interactive operations in a manner that

allows each user to shift back and forth between hardware emulation and software simulation to discover and eliminate problems in the IC design. Applicant respectfully points out that Isaka provides an IP conference telephone system and has nothing to do with IC design or emulation or simulation thereof. There is no motivation to apply the teachings of Lin to Isaka based on the benefits set forth by the Examiner because these benefits relate to the modeling of a circuit design and have no relation at all to IP communications.

As to claim 5, applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

As to claims 9-10, 14, and 24-25, the Examiner asserts that these claims do not teach or define any new element above claims 1-2 and the Examiner rejects these claims for similar reasons as claim 3. Applicant likewise traverses the rejections for similar reasons.

Applicant has cancelled all claims and presents new claims 26-50. Applicant respectfully requests that the Examiner withdraw the rejection of claims 4-5, 9-10, 14, and 24-25 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Iwama, in view of Onishi, and further in view of Lin.

6. The Examiner rejects claims 16-18 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Isaka (US 6,654,455) in view of Iwama et al. (US 6,600,735), and further in view of Lin et al. (US 6,651,225).

As to claim 16, the Examiner asserts that Isaka teaches a host system and a line card. The Examiner admits that Isaka does not teach a buffer memory. The Examiner asserts that Iwama teaches a buffer memory and that it would have been obvious to combine the teachings of Isaka and Iwama to achieve the claimed device. The Examiner admits that Isaka does not teach a

multicast hardware accelerator. The Examiner asserts that Lin teaches a hardware accelerator and that it would have been obvious to combine the teachings of Isaka, Iwama, and Lin to achieve the claimed device.

Applicant has amended claim 16 to more clearly distinguish the claimed invention from the teachings of Isaka, Iwama, and Lin.

The Examiner reads the claimed element of a host system on the multicast router 70 taught by Isaka. The Examiner asserts that Isaka teaches a line card citing the teaching of at least three telephone terminal systems connected to a conference trunk, the multicast router 70 being substituted for the conference trunk 24, and a CPU 40 included in each of the telephone terminal systems identifying a packet meant for the telephone. Col. 7, lines 26-32, and 60-65. The Examiner appears not to consider that what is claimed is a network device that includes the claimed elements. The Examiner has cited element taught by Isaka that are distributed and coupled by an IP network. Applicant respectfully submits that Isaka does not teach or suggest these elements comprising a single network device as claimed. To more clearly point out and claim the network device, applicant has amended the claim to include elements of inter-relationship and cooperation between the host system, the line card, and a buffer memory. As amended it is clear that the line card is able to multicast voice data stored in the buffer memory to a plurality of ports provided by the line card as selected by a single voice packet received from the host system. Isaka teaches a system where a conference trunk adds and subtracts packetized voice signals from a plurality of telephones in an IP-PBX to allow a conference between telephones in the IP-PBX. Nothing in Isaka teaches or suggests that the host system causes the line card to multicast to its ports responsive to a single voice packet provided by the host system.

The Examiner admits that Isaka does not teach a buffer memory. The Examiner asserts that Iwama teaches a buffer memory citing a storage device 1802 in Figure 9. Iwama teaches a method for managing communication bandwidth. Iwama teaches that the storage device is for storing indexes representing the performance of the network. Col. 14, lines 54-64. Nothing in Iwama teaches or suggests storing voice data extracted from the network packet by the host system as now claimed.

The Examiner asserts that one would have been motivated to modify Isaka to introduce the buffer of Iwama to retain information as close to the input/output loop as possible to reduce access time. Applicant fails to see where such a motivation to combine the references is found in either of the references. Further, one would expect that buffering would increase the access time as compared to the unbuffered system taught by Isaka. In any event, even if Isaka was modified to introduce the buffer of Iwama, the resulting system would still not provide a buffer memory as now claimed.

The Examiner admits that Isaka does not teach a multicast hardware accelerator. The Examiner asserts that Lin teaches a hardware accelerator citing item 120 of Figure 2. Lin teaches a dynamic logic evaluation system. Applicant respectfully submits that Lin is non-analogous art and that one of ordinary skill in the art would not be motivated to consider the teachings of Lin in connection with voice communication.

The hardware accelerator taught by Lin is a modeling of a circuit design where the model is implemented in hardware, such as a FPGA. The hardware model is used as an alternative to software simulation for portions of the cycles being modeled for the circuit design. Col. 15, line 57, through Col. 19, line 14. Nothing in Lin teaches or suggests "a multicast hardware

accelerator to multicast the voice data stored in the buffer memory to ports selected from the plurality of ports by a single voice packet received from the host system" as now claimed.

The Examiner asserts that one would have been motivated to modify Isaka to provide the hardware accelerator of Lin to allow multiple users doing interactive operations in a manner that allows each user to shift back and forth between hardware emulation and software simulation to discover and eliminate problems in the IC design. Applicant respectfully points out that Isaka provides an IP conference telephone system and has nothing to do with IC design or emulation or simulation thereof. There is no motivation to apply the teachings of Lin to Isaka based on the benefits set forth by the Examiner because these benefits relate to the modeling of a circuit design and have no relation at all to IP communications.

As to claim 17, applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

As to claim 18, the Examiner asserts that Isaka teaches the host system is to send a packet relating to the data stored in the buffer memory, the packet includes descriptor fields used to multicast the data stored in the buffer memory. Applicant has amended claim 18 in view of the amendments to claim 16. Since the Examiner has admitted that Isaka fails to teach a buffer memory in connection with claim 16, applicant fails to understand how Isaka can disclose a packet to multicast data stored in a buffer memory. The portions of Isaka cited by the Examiner appear merely to describe that packets including voice data are sent to an IP network where a CPU in an attached telephone identifies those packets meant for the telephone. This does not disclose a voice packet that enables multicasting of voice data that is stored in a buffer memory as now claimed.

As to claim 20, applicant has cancelled the claim.

Applicant has cancelled all claims and presents new claims 26-50. Applicant respectfully requests that the Examiner withdraw the rejection of claims 16-18 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Iwama, and further in view of Lin.

New Claims

Claim 26 is patentably distinguished from Isaka and Iwama at least by separating voice data to be stored in a memory and using a voice packet having digital signal processing (DSP) mask field to select ports on a line card on which the voice data should be multicast.

In great contrast to the claimed invention, Isaka teaches a method where a multicast IP address is registered for a conference connection. The network recognizes that particular telephones belong to the multicast group designated by the multicast IP address by reference to IGMP report packets. Thus the network forwards voice packets to the particular telephones that belong to the multicast group by recognizing the multicast IP address as one previously memorized to designate the particular telephones. Col. 8, lines 28-55. This is entirely unlike the claimed invention that provides a DSP mask field in the voice packet that selects the ports on a line card on which the voice data that is stored in a memory rather than in the packet should be multicast.

Iwama teaches an Internet telephone connection method wherein a communication bandwidth is managed by using a bandwidth controller and gateway devices and voice relay routers monitor communication quality under bandwidth reservation. Iwama does not teach or suggest multicasting voice packets and therefore cannot teach or suggest a method for selecting ports on a line card as part of a method of performing voice multicasting with a router. Claims 31, 36, 41, and 46 are similarly distinguished from Isaka and Iwama.

As to claims 27, 32, 37, 42, and 47, these claims include the element of the DSP mask field comprising a bit field map having a plurality of bits in which each one of the plurality of bits selects one of the corresponding plurality of ports. Neither Isaka nor Iwama, alone or in combination, teach or suggest the use of a bit field map to select ports on a line card. In the rejection of cancelled claims 3, 8, 13, and 23, the Examiner asserted that Onishi teaches descriptor fields that include a memory pointer field, status field, mask field, or a data length field citing figure 14 and column 7, line 66, through column 8, line 10, where Onishi discloses a routing table including an IP address of a destination network, subnet mask data, and a pointer field for a next entry. Applicant respectfully submits that nothing in Onishi teaches or suggests "a bit field map having a plurality of bits in which each one of the plurality of bits selects one of the corresponding plurality of ports" as now claimed because selecting ports on a line card by single bits is entirely unlike using subnet mask data to identify a subnet of a destination network.

As to claims 28, 33, 38, 43, and 48, these claims include the element of the voice packet including descriptor fields for retrieving the voice data from the memory for multicasting. In the rejection of cancelled claims 3, 8, 13, and 23, the Examiner asserted that Onishi teaches descriptor fields that include a memory pointer field, status field, mask field, or a data length field citing figure 14 and column 7, line 66, through column 8, line 10, where Onishi discloses a routing table including an IP address of a destination network, subnet mask data, and a pointer field for a next entry. Applicant respectfully submits that nothing in Onishi teaches or suggests "descriptor fields for retrieving the voice data from the memory for multicasting" as now claimed because retrieving voice data from a memory for multicasting is entirely unlike finding the next entry in a routing table.

As to claims 29, 34, 39, 44, and 49, these claims include the element of multicasting the voice data without duplicating packets. None of the prior art of record teaches or suggests a method of multicasting voice data without duplicating packets.

As discussed above, the prior art references cited by the Examiner fail to teach or suggest each and every element of the newly presented claims. Further, even if the cited prior art references were considered to teach all claimed elements, there is no teaching or suggestion in the references themselves or generally in the art at the time the application was filed that suggests combining the elements in the way now claimed without the use of impermissible hindsight based on the applicant's own disclosure. Finally, even if the elements of the cited prior art references were combined, the combination would still fail to provide the structure and function of the claimed invention.

Conclusion

Applicant reserves all rights with respect to the applicability of the doctrine of equivalents. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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By _____

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